IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15472US02

In re Application of:	)	
	)	**Electronically Filed**
Pai	)	
	)	**Date: September 15, 2008**
Serial No.: 10/816,320	)	
	)	
Filing Date: 4/1/2004	)	
	)	
Examiner: Holder	)	
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Confirmation No.: 9138	)	
	)	
Art Unit No. 2621	)	
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This amendment is filed in response to the Office Action mailed 8/12/2008.

REMARKS

Claims 1, 2, 4-9, 11-15, and 17-20 are presently pending. Claims 3, 10, and 16 are cancelled without prejudice. Assignee respectfully requests pre-appeal review of the rejection.

Claims 1 and 13 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise in view of Kawaharada. Claim 1 recites, among other limitations, "wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input". Examiner has indicated that Wise does not specifically teach this limitation. Office Action at 3.

However, Examiner has indicated that Kawaharada teaches that "the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input. [fig. 9-1; fig. 9-2; fig. 1; 0106; 0108 motion vectors are counted and the predictive determines the picture type combination is equivalent to validity determiner.]". Office Action at 3. As an initial matter, it appears to Assignee that Examiner meant to say "[fig. 9-1; fig. 9-2; fig. 1; 0106; 0108 motion vectors are counted and the predict***or*** determines the picture type***. The*** combination is equivalent to validity determiner.]". If the foregoing is not the case, Assignee respectfully requests that Examiner clarify.

Assignee respectfully traverses the rejection because Kawaharada, including paragraphs 106 and 108, and Figures 9-1, 9-2, does not even teach validating parameters, much less "the logic determines whether the parameters received

by the input are valid based on the picture type indicator and the number of motion vectors received by the input".

Moreover, even if Kawaharada teaches that "motion vectors are counted" and "determines the picture type", and Wise teaches "logic for determining whether the parameters received by the input are valid", Assignee respectfully submits that the combination of Wise and Kawaharada would still not teach that the logic determines whether parameters received by the input are valid "***based on*** the picture type indicator and the number of motion vectors received by the input." Neither Wise nor Kawaharada teach any way that parameters can be validated "based on the picture type indicator and the number of motion vectors".

Assignee also traverses that it would have been obvious to combine Kawaharada with Wise for "allowing for improved coding and reproduction". It is first noted that Wise is directed to "Multistandard Video Decoder and Decompression System for Processing Encoded Bit Streams including a Video Formatter and Methods Relating Thereto". In contrast, Kawaharada is directed to "Moving Picture Compression/Coding Apparatus and Motion Vector Detection Method". It is submitted that incorporation of Kawaharada into Wise would not improve reproduction because Kawaharada is directed to encoding. Additionally, since Wise already receives "encoded bit streams" as input, one skilled in the art would not seek to modify Wise to include "Moving Picture Compression/Coding Apparatus".

Accordingly, Assignee respectfully traverses the rejection to claims 1 and 13, and requests that Examiner withdraw them, as well as the rejections to dependent claims 2, 4-9, 11-15, and 17-20.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being

obvious from the combination of Wise in view of Kawaharada and further in view of Kim. Claim 5 recites, among other limitations, “wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector”.

Examiner has indicated that the combination of Wise, Kawaharada, and Kim teaches the foregoing, at [Kim – Abstract; col. 1 lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6, Lines 8-12]. As noted in the response to the previous office action, although in Kim, Abstract, the “motion vector decoder” includes a number of things, e.g., “a parameter delay block”, “a motion vector residual block”, “motion vector code table”, etc., Kim abstract does not teach anything that “comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector”.

Moreover, Kim, Col. 6, Lines 8-12 recites that:

> The vlc[10:0], shown in FIG. 2(e), is a MV value variable length coded by the encoder and is received by the MV residual block 11 and the MV code table block. Since maximum of 11 data bits may be produced through the VLC, the vlc[10:0] has a length of 11 bits and is the most significant bit (msb). The msb value may or may not be sent by the encoder and if sent, one or all eight values may be sent.

(Emphasis Added). It is noted that Kim does not teach that “vlc[10:0]” “comprises one or more bits, each of which are

associated with a corresponding one of the one or more motion vector registers". Moreover, it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44. Thus vlc[10:0] does not "comprise[s] one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Although, Examiner has also indicated that "Kim discloses 8 bit number in the residual value. [col. 5 line 57 - col. 6, lines 20]". Office Action at 2. Assignee respectfully submits that "wherein the control register comprises one or more bits, *each of which are associated with a corresponding one or the one or more motion vector registers*, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector" does not read on "8 bit number in the residual value." Accordingly, Assignee respectfully maintains traverse of the rejection of claim 5 and requests that Examiner withdraw it.

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as obvious from the combination of Wise (modified by Kawaharada and Kim). Claim 6 recites, among other limitations, "wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state". Claim 7 recites, among other limitations, "wherein the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less

than two of the one or more bits are in the particular state".

Assignee traverses the rejections to claims 6 and 7 because Examiner's rejection in the final office action is conclusory and not supported by any citation to Wise, Kim, or Kawaharada that supports Examiner's assertion. In the previous office action, Examiner made reference to "Wise- pg. 51 0682 Table A.3.2; Pg. 13, 0160, 0165; pg. 18, 0220-0221; pg. 117 1595; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12." Assignee respectfully submits that none of the foregoing citations even mention the conditions "that the type of picture is an (I/B)-picture", "(any/less than two) one of the one or more bits are in the particular state". Accordingly, Assignee respectfully traverses the rejections to claims 6 and 7 and requests that Examiner withdraw it.

CONCLUSION

For at least the foregoing reasons, Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: September 15, 2008

Respectfully submitted,

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 15472US02

I hereby certify that this correspondence is being electronically filed with United States Patent and Trademark Office

on September 15, 2008

Signature /Mirut P. Dalal/

Typed or printed Name Mirut P. Dalal

Application Number	Filed
10/816,320	04/01/2004

First Named Inventor: Pasqualino et al.

Art Unit	Examiner
2621	Holder

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest.
  See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
  (Form PTO/SB/96)
- ☒ attorney or agent of record.
  Registration number 44,052 .
- ☐ attorney or agent acting under 37 CFR 1.34.
  Registration number if acting under 37 CFR 1.34 .

/Mirut P. Dalal/
Signature

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Typed or printed name

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Telephone number

September 15, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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